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MZ104

user manual V4.01

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www.tri-m.com.

WARNING

- A working knowledge of electronics and PC-technology is required to use this product.
- Pay attention to electrostatic discharges. Use a CMOS protected workplace.
- Disconnect power source when connecting any cables or devices.

This is a high-technology product.
A working knowledge of electronics and PC-technology is required!

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1.1. GENERAL DESCRIPTION

The MZ104 is a PC/104 compliant system controller measuring just 3.55 inches by 3.775 inches. The MZ104 offers the quickest route of integrating a full x86 AT-compatible computer into your embedded control application using the PC/104 form factor. In addition, the built-in peripherals minimize the number of additional modules required. By combining the system hardware, I/O, software (integrated RTOS image) and solid-state mass storage, the MZ104 lowers your exposure to possible development risks, costs and significantly reduces your time-to-market.

The MZ104's full compatibility with the popular PC/104 embedded expansion bus, which allows you to easily integrate the widest selection of low-cost hardware peripherals. The numerous features provide an ideal price/performance solution.

1.2 SPECIFICATIONS

586 CPU

- 32-bit CPU core operating at 133[1], 100, 66 and 33MHz
- 8K byte Level 1 cache, write back and write through support
- Floating point unit

PC Core Logic with PCI enhancement

- 32 bit 33MHz PCI rev 2.1 compliant "Northbridge" and "Southbridge"
- AT-compatible DMA controllers, interrupt controllers, timer/counters
- AT keyboard controller and Real-time clock

Memory

- Synchronous DRAM support
- Onboard 144-pin DIMM socket for up to 64MB SDRAM

Universal Serial Bus

- One independent USB interface, USB 1.1 and OpenHCL compliant
- PCI bus master burst reads and writes
- Over current and power control support

Serial Ports

- Two 16550-compatible RS232 serial ports
- Baud rates up to 115.2 K baud

Parallel Ports

- One enhanced bi-directional parallel port
- Supports SPP, ECP and EPP

Keyboard/Mouse Interface

- Supports AT keyboard and PS/2 mouse

FDD Interface

- Supports two floppy disk drives

Enhanced IDE Interface

- One enhanced IDE channel, supports up to two drives (master/slave)
- PCI bus master burst reads and writes
- Ultra DMA and PIO modes (1-4) support

Power Management

- I/O traps and idle timers for peripheral power management
- Hardware and software CPU suspend mode support

[1] 133MHz is overclocking the CPU and performance is not guaranteed. Additional cooling is required.

Solid State Flash Storage

- One 32-pin DIP socket supports M-System DiskOnChip 2000 and DiskOnChip Millennium

Expansion BUS - ISA PC/104 signals

- Fully compliant 16-bit PC/104 Expansion BUS

Electrical Specifications

- Support for low-power modes via BIOS APM features

		MEMORY SIZE			
		8 MB	**16 MB**	**32 MB**	**64 MB**
SPEED	**33 MHz**	2.8 W	2.7 W	2.8W	2.9W
	66 MHz	3.1 W	3.0 W	3.1W	3.2W
	100 MHz	3.4 W	3.3 W	3.4 W	3.4 W

Table 1: MZ104+ Power Consumption (Watts)

Note: Power consumption figure is averaged with APM disabled.

Mechanical/Environmental

- PC/104 form factor compliant, 3.55" x 3.775 x 0.9" (90mm x 96mm x 23mm)
- Standard PC/104 16-bit stackthrough connector for PC/104-compliant modules
- Standard ribbon cable connectors for IDE, serial, parallel and utilities.
- ZFx86 Case Temperature (33, 66, 100MHz operation): -40° to 185°F (-40° to 85°C)[2]
- ZFx86 Case Temperature (133MHz operation): -4° to 158F (-20° to 70C)
- Storage temperature: -67° to 185°F (-55° to 85°C)
- Weight: 0.15 lb. (70G)

[2] Extended temperature memory available upon request.

1.3 EMBEDDED FEATURES

FailSafe Boot ROM

- 12Kbyte BIOS update ROM (BUR) to allow flash BIOS install or upgrade
- Provides permanent and fail-safe mechanism to update software under all adverse conditions
- External Fail-Safe™ Code may be installed in optional 8 – 32Kb SEEPROM inserted into socket IC1

Z-Tag Interface

- High speed interface to download software
- Uses floppy interface when "Drive Select" signal is inactive
- Communication protocol compatible with serial EEPROMs
- Z-tag programming tool allows easy field upgrade

Dual Watchdog Timer

- Software and hardware control of WatchDog Timer event
- 16-bit counter primary watch dog connected to WSIRQ/NMI/SMI, reset by WDT input
- Second 8-bit counter connect to H/W reset line, enabled by primary counter output

Software included

- Phoenix embedded PC BIOS – 100% X86 Compatible

Software Compatibility

- Linux
- MSDOS 3.X, 4.X, 5.X, 6.X, DRDOS
- Win95/98/NT
- most PC-Compatible RTOS
- WindRiver VxWorks RTOS

CHAPTER 2 - INSTALLATION

2.1 LOCATING THE CONNECTORS & JUMPERS

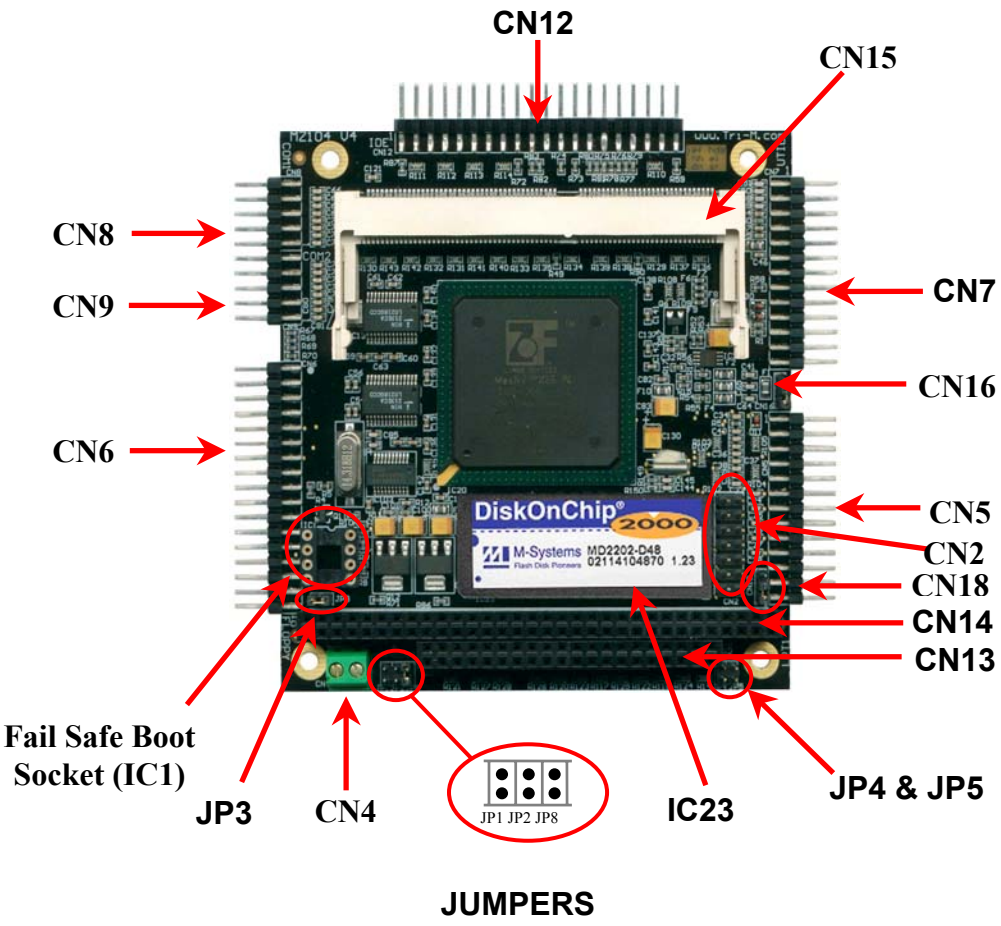

Figure 1: Jumper/Connector Location

2.2 PIN-1 LOCATION

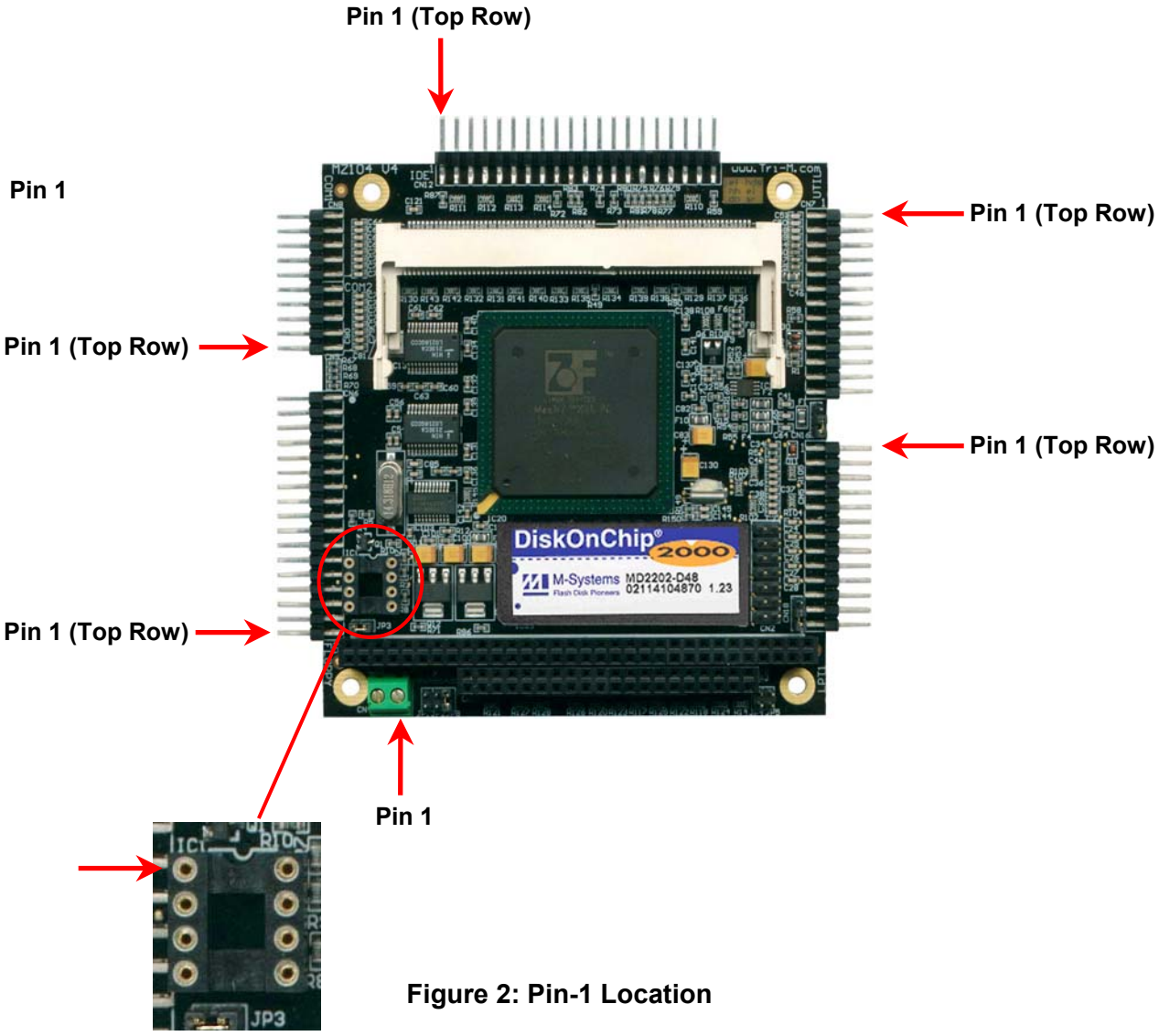

Figure 2: Pin-1 Location

2.3 MZ104 CABLE SETS (OPTIONAL)

CABLE SET 1 (PART# CABLESET1-MZ104)

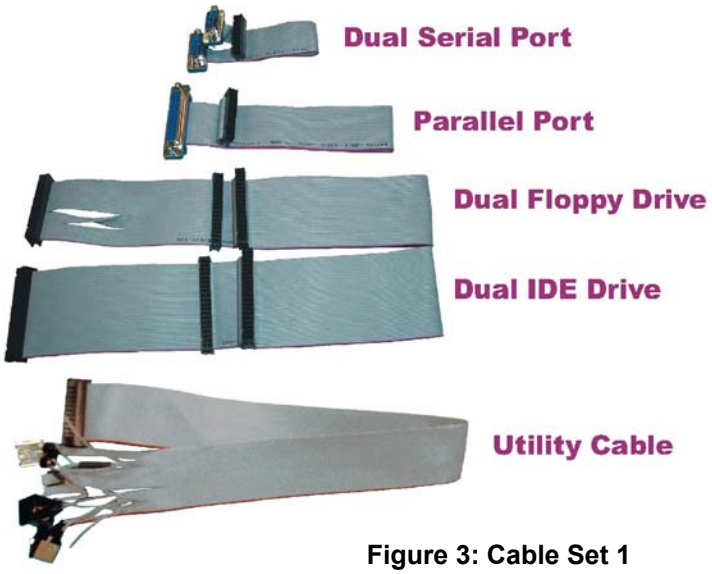

Figure 3: Cable Set 1

CABLE SET 2 (PART# CABLESET2-MZ104)

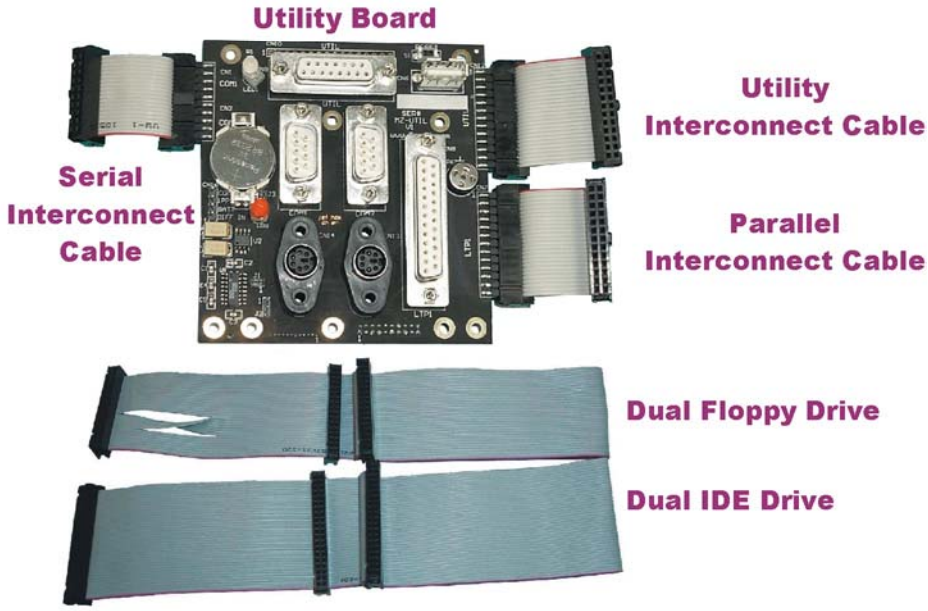

Figure 4: Cable Set 2

2.4 MZ104 Utility Board (Optional)

The optional MZ104 Utility Board, the UTIL104, provides a convenient means to connect peripheral devices to the MZ104 embedded CPU module. It provides connectors to interface to standard PC peripherals. In addition, the UTIL104 provides some input/output functionality such as status LED and hardware-reset switch. For applications requiring a GPS receiver, the UTIL104 also acts as a carrier board to mate with several models of RoyalTek GPS receivers available from Tri-M Systems.

Figure 5: UTIL104 interfaced with an MZ104

The MZ104 Utility Board can be interfaced to the MZ104 CPU module via three short flat ribbon cables provided with optional CABLESET2-MZ104 (see figure 4) available from Tri-M Systems. The UTIL104 can be mounted above the MZ104 with PC/104 stand offs.

		Connect Between	
Cable	**Function**	**MZ104**	**Utility Board**
1" 20-pin (2x10) IDC ribbon cable	COM1/COM2	CN8/CN9	CN1/CN2
1" 26-pin (2x13) IDC ribbon cable	Parallel	CN5	CN7
1" 26-pin (2x13) IDC ribbon cable	Utility	CN7	CN12

Table 2: UTIL104+ Interface

The UTIL104 utility board supports the Royaltek REB2000/2100 series as well as the REB12R series GPS receivers. A 12-position single-row female socket is provided for the REB2000/2100 series receiver while a 20-position dual-row female socket is provided for the REB12R series receiver. Power is provided to the UTIL104 board through connector CN7 on the MZ104. No separate power source is required.

Note: J1 must be installed in order to route GPS output to CN3. Make sure to disconnect cable between CN1/CN2 and CN8 of MZ104 to make COM1 and COM2 available.

CHAPTER 3 – JUMPERS

Jumpers are provided on the MZ104 to set the System, PCI and CPU clocks speed as well as to select the BUR/Boot ROM.

Jumpers	
Label	**Function**
JP1, JP2	Clock multiplier select
JP3,JP4,JP5	PCI & System clock select
JP8	BUR/Boot ROM select

Table 3: List of Jumpers

3.1 CLOCK MULTIPLIER SELECT (JP1, JP2)

The clock multiplier selection jumper sets the clock for the MZ104 CPU core. The CPU operating speed is determined by:

CPU frequency ratio * System clock (33MHz)

For example, using 2X ratio, the CPU speed will be (2 * 33) = 66MHz

CPU Frequency ratio	JP1	JP2
1X	ON	ON
2X	OFF	ON
3X	OFF	OFF

Table 4: Clock Multiplier Select

3.2 SYSTEM CLOCK & PCI CLOCK SELECT (JP3, JP4, JP5)

Jumper JP3, JP4 and JP5 set the speed of the PCI bus and the system clock.

System Clock	PCI Clock	JP3	JP4	JP5
33Mhz	33Mhz	ON	OFF	OFF
66Mhz	33Mhz	OFF	ON	ON

Table 5: System Clock & PCI Clock Select

For example, to setup MZ104 with 33Mhz PCI, 66Mhz System and 66Mhz CPU clock:

JP1	JP2	JP3	JP4	JP5
ON	ON	OFF	ON	ON

To setup MZ104 with 33Mhz PCI, 33Mhz System and 100Mhz CPU clock:

JP1	JP2	JP3	JP4	JP5
OFF	OFF	ON	OFF	OFF

3.3 BUR/BOOT ROM SELECT (JP8)

JP8 allows the MZ104 to boot from standard BIOS or BUR. If boot ROM mode is selected, the MZ104 will startup normally by executing the BIOS code and transfer control to a boot device. If BUR mode is selected, the MZ104 will execute the BUR code to update the flash BIOS using the Z-Tag interface. It also provides an elementary debugger console functionality through COM1. For details of Z-Tag and BUR operation, see the MachZ data book see the ZFx86 Data Book provided on the MZ104 Quickstart CD or available for download at www.ZFMicro.com.

BUR /BOOT ROM select (JP8)		
JP8	BUR Mode OFF	Boot ROM* ON

Table 6: BUR/BOOT ROM Select

3.4 ZTAG TOOL SELECT (CN18)

CN18 should have a jumper shunt installed between CN18-2 and CN18-3 for proper operation of the “Z-Tag Dongle”.

CHAPTER 4 - CONNECTORS

Connectors on the MZ104 are provided to interface external devices such as a hard disk drive, floppy drive, and keyboard.

MZ104 Connector List	
Connecotor Label	**Function**
CN2	Z-tag connector for field flash update or user code execution
CN4	External power connector
CN5	Parallel port connector
CN6	Floppy drive connector
CN7	Utility connector for keyboard, mouse, USB, battery and speaker
CN8	COM2 serial port connector
CN9	COM1 serial port connector
CN12	IDE drive connector
CN13	PC104 connector (40-pin)
CN14	PC104 connector (64-pin)
CN15	SO-DIMM memory socket
CN16	Watchdog trigger source
IC23	DiskOnChip socket

Table 7: MZ104 Connector List

Note: Pin-1 of each connector on the MZ104 is designated by a small, white dot on the PCB. Pin-1 of the connector should line up with pin-1 of the corresponding mating connector on the cable. Please refer to "Figure 2" for pin-1 location.

4.1 Z-TAG CONNECTOR (CN2)

The Z-Tag connector (CN2) is a 14-pin connector that interfaces with the Z-Tag Dongle allowing for easy field flash updates or user code execution. Please refer to the Z-Tag and BUR chapter of the ZFx86 Data Book for complete details. A *Z-Tag Manager* utility program and manual are provided on the MZ104 Quickstart CD and are available for download at www.ZFMicro.com. The Z-Tag Dongle, part number ZFx86DONGLE-1, is available from Tri-M Systems.

4.2 EXTERNAL POWER (CN4)

The MZ104 can be powered by supplying 5VDC and ground to CN4. Alternatively, the MZ104+ can be powered by supplying 5VDC through the 16-bit PC104 connector (CN13) with a PC104 power supply such as the Tri-M Engineering HE104 or HESC-104.

External Power (CN4)	
Pin Number	**Signal**
1	Vcc +5V
2	GND

Table 8: External Power Connector

4.3 PARALLEL INTERFACE (CN5)

The MZ104 parallel port is fully compatible with the PC/AT parallel port. In the extended mode, it functions as a PS/2-like bi-directional port. In Extended Capabilities Port (ECP) mode, it is IEEE 1284 compliant, including level 2.

The parallel ports uses the following PC resources when enabled:

Parallel Port	Typical Usage	I/O Address	Standard Interrupt
Parallel 1	LPT1	378H – 37 Fh	IRQ7

Table 9: Parallel Port Resources

The default interrupt for parallel port LPT1 is IRQ7. The parallel port output signals provide up to 14mA drive current. RC filters are provided for noise suppression. The parallel port signals appear on CN5, a dual-row ribbon-cable pin edge connector. The port may be cabled to appear on a standard PC DB-25 connector. A DB-25 connector and cable are provided for this purpose in the optional MZ104 cable kit. The following table shows the parallel port signals appearing on CN5 and the equivalent pinout on a DB-25 connector.

CN5	DB-25 Pin	Signal	Function	In/Out	CN5	DB-25 Pin	Signal	Function	In/Out
1	1	STRB-	Output data strobe	OUT	2	14	AUTOFD-	Auto feed	OUT
3	2	PD0	Data bit 0	I/O	4	15	ERR-	Printer error	IN
5	3	PD1	Data bit 1	I/O	6	16	INIT-	Initialize printer	OUT
7	4	PD2	Data bit 2	I/O	8	17	SLCTIN-	Selects printer	OUT
9	5	PD3	Data bit 3	I/O	10	18	GND	Signal Ground	N/A
11	6	PD4	Data bit 4	I/O	12	19	GND	Signal Ground	N/A
13	7	PD5	Data bit 5	I/O	14	20	GND	Signal Ground	N/A
15	8	PD6	Data bit 6	I/O	16	21	GND	Signal Ground	N/A
17	9	PD7	Data bit 7	I/O	18	22	GND	Signal Ground	N/A
19	10	ACK-	Character acknowledged	IN	20	23	GND	Signal Ground	N/A
21	11	BUSY	Printer busy	IN	22	24	GND	Signal Ground	N/A
23	12	PE	Out of paper	IN	24	25	GND	Signal Ground	N/A
25	13	SLCT	Printer selected	IN	26	N/A	GND	Signal Ground	N/A

Table 10: Parallel Port Connections

Note: CN5 is an edge mounted PCB connector with odd number pins located on the "top", and even number pins on the "bottom".

4.4 FLOPPY INTERFACE (CN6)

The floppy interface provides the signal to control two 3 ½" and/or 5 ¼" floppy drives. A 34-pin daisy-chain drive connector cable is required for a dual-drive system. The default interrupt request for the floppy interface is IRQ6.

Pin	Signal	Pin	Signal
1~33 (odd)	GND	2	High Density
4	Unused	6	Unused
8	Index	10	Motor Enable
12	Drive Select B	14	Drive Select A
16	Motor Enable B	18	Direction
20	Step Pulse	22	Write Data
24	Write Enable	26	Track 0
28	Write Protect	30	Read Data
32	Select Protect	34	Disk Change

Table 11: Floppy Interface

4.5 UTILITY PORT (CN7)

The utility connector provides the following inputs and outputs:

- Keyboard
- PS/2 mouse
- Universal Serial Bus
- Infrared port
- Speaker
- CMOS backup battery
- Watchdog trigger source
- Hardware reset
- Hard drive LED

Signals on CN7 can be terminated using the optional MZ104 utility board, the UTIL104. The UTIL104 provides the appropriate connectors for all the signals.

Utility Connector (CN7)		
Pin	**Signal**	**Function**
1	KBDATA	Keyboard data
2	KBCLK	Keyboard clock
3	MDATA	P/S 2 mouse data
4	MCLK	P/S2 mouse clock
5	KBLOCK	Keyboard lock
6	SPKOUT	Speaker output
7, 8	GND	Ground
9, 10	KBMPWR	+5V
11	NC	No connection
12	WDEXT	External trigger source for watchdog timer
13	IRTx	Infrared transmit
14	IRRx	Infrared receive
15	RESET	Hardware reset
16	HDDLEDOUT	Hard drive LED output (8mA source)
17	NC	No connection
18	NC	No connection
19	VCC-EXTBAT	RTC Backup battery +V terminal (3.6V)
20	GND	Ground
21	SCL	SMBus clock
22	SDA	SMBus data
23	USBVCC1	USB port 1 power
24	USBD1F-	USB port 1 data minus
25	USBD1F+	USB port 1 data plus
26	USBGND1	USB port 1 ground

Table 12: Utility connector

4.6 SERIAL INTERFACES (CN8, CN9)

The MZ104 provides two PC-compatible asynchronous serial ports. Typically, DOS and Windows treat the serial ports as COM1, and COM2. Standard system resources are allocated to the serial ports:

Serial Port	Typical Usage	I/O Address	Standard Interrupt
Serial 1 (CN8)	COM1	3F8h–3FFh	IRQ4
Serial 2 (CN9)	COM2	2F8h–2FFh	IRQ3

Table 13: Serial Port Resources

Serial 1 and Serial 2 ports can be disabled using BIOS SETUP. When disabled, the port's I/O address is made available for other expansion devices on the 16-bit BUS.

COM1 (CN8) Details

A full complement of input and output handshaking lines is supplied by serial port COM1 and COM2. These signals are at standard RS232C levels. The RS232C level converters provide the required RS232C voltage levels with internal +5 volt to ±9 volt converters.

CN8	DB-9 Pin	Signal	Function	In/Out	CN8	DB-9 Pin	Signal	Function	In/Out
1	1	DCD1	Serial 1 Data Carrier Detect	IN	2	6	DSR1	Serial 1 Data Set Ready	IN
3	2	RXD1	Serial 1 Receive Data	IN	4	7	RTS1	Serial 1 Request To Send	OUT
5	3	TXD1	Serial 1 Transmit Data	OUT	6	8	CTS1	Serial 1 Clear To Send	IN
7	4	DTR1	Serial 1 Data Terminal Ready	OUT	8	9	RI1	Serial 1 Ring Indicator	IN
9	5	GND	Signal Ground		10		N/C	No connection	

Table 14: Serial Port COM1 Connection

COM2 (CN9) Details

CN9	DB-9 Pin	Signal	Function	In/Out	CN9	DB-9 Pin	Signal	Function	In/Out
1	1	DCD1	Serial 1 Data Carrier Detect	IN	2	6	DSR1	Serial 1 Data Set Ready	IN
3	2	RXD1	Serial 1 Receive Data	IN	4	7	RTS1	Serial 1 Request To Send	OUT
5	3	TXD1	Serial 1 Transmit Data	OUT	6	8	CTS1	Serial 1 Clear To Send	IN
7	4	DTR1	Serial 1 Data Terminal Ready	OUT	8	9	RI1	Serial 1 Ring Indicator	IN
9	5	GND	Signal Ground		10		N/C	No connection	

Table 15: Serial Port COM2 Connection

Note: CN8 and CN9 are an edge mounted PCB connector with odd number pins located on the "top", and even number pins on the "bottom". Pin-1 is designated by a white dot on the PCB.

4.7 IDE INTERFACE (CN12)

The MZ104 has a PCI bus mastering ATA-4 compatible IDE controller. The IDE controller supports Ultra DMA, Multi-word DMA, and all Programmed I/O (PIO) modes. Up to two drives can be connected, in a master-slave arrangement. Generally, the first hard disk drive (master) will appear as the C drive to DOS. The second drive, if attached, will appear as D.

Resource	Function
I/O Address (1F0h-1F7h)	Hard Disk Interface
IRQ14	Interrupt

Table 16: Hard Disk Resources

Use SETUP to auto-detect your attached hard drives. For further details about setting up IDE hard disk parameters See the SETUP description in the BIOS manual provided on the MZ104 Quickstart CD or available for download at www.ZFMicro.com.

IDE Interface (CN12)							
Pin	**Signal Name**	**Function**	**In/Out**	**Pin**	**Signal Name**	**Function**	**In/Out**
1	HDRESET-	Reset signal from host	OUT	2	GND	Ground	
3	HDD07	Data bit 7	I/O	4	HDD08	Data bit 8	I/O
5	HDD06	Data bit 6	I/O	6	HDD09	Data bit 9	I/O
7	HDD05	Data bit 5	I/O	8	HDD10	Data bit 10	I/O
9	HDD04	Data bit 4	I/O	10	HDD11	Data bit 11	I/O
11	HDD03	Data bit 3	I/O	12	HDD12	Data bit 12	I/O
13	HDD02	Data bit 2	I/O	14	HDD13	Data bit 13	I/O
15	HDD01	Data bit 1	I/O	16	HDD14	Data bit 14	I/O
17	HDD00	Data bit 0	I/O	18	HDD15	Data bit 15	I/O
19	GND	Ground		20	KEY	Keyed pin	N/C
21	IDEPDREQ	DMA 0 Request	OUT	22	GND	Ground	
23	HDIOW-	Write strobe	OUT	24	GND	Ground	
25	HDIOR-	Read strobe	OUT	26	GND	Ground	
27	HDRDY	I/O Channel Ready	IN	28	GND	Ground	
29	IDEPDACK	DMA 0 Acknowledge	IN	30	GND	Ground	
31	IRQ14	Drive interrupt request	IN	32	IOCS16-	I/O Chip Select 16	In
33	HDA1	IDE Address 1	Out	34	RSVD	Reserved	N/C
35	HDA0	IDE Address 1	Out	36	HDA2	IDE Address 2	Out
37	HDCS0-	IDE Chip Select 0	Out	38	HDCS1-	IDE Chip Select 1	Out
39	LEDIN-			40	GND	Ground	

Table 17: IDE Drive Interface

NOTE: For maximum reliability, IDE drive cables should be limited to 18 inches or less in length.

4.8 PC/104 CONNECTOR (CN14 AND CN13)

Both CN13 and CN14 provide the flexibility to attach PC/104 expansion modules to the MZ104. These modules perform the functions of traditional add-in card in a PC environment. All data, address and control signals are able to sink 10mA and source 8mA.

8-bit, 64-pin Connector (CN14)

PC/104 8-bit Connector (CN14)			
Pin #	**Signal**	**Pin #**	**Signal**
A1	/IOCHCK	B1	GND
A2	SD7	B2	RESETDRV
A3	SD6	B3	+5V
A4	SD5	B4	IRQ9
A5	SD4	B5	-5V
A6	SD3	B6	DRQ2
A7	SD2	B7	-12V
A8	SD1	B8	/0WS
A9	SD0	B9	+12V
A10	IOCHRDY	B10	GND(*)
A11	AEN	B11	/SMEMW
A12	SA19	B12	/SMEMR
A13	SA18	B13	/IOW
A14	SA17	B14	/IOR
A15	SA16	B15	/DACK3
A16	SA15	B16	DRQ3
A17	SA14	B17	/DACK1
A18	SA13	B18	DRQ1
A19	SA12	B19	/REFRESH
A20	SA11	B20	SYSCLK
A21	SA10	B21	IRQ7
A22	SA9	B22	N/A
A23	SA8	B23	IRQ5
A24	SA7	B24	IRQ4
A25	SA6	B25	IRQ3
A26	SA5	B26	/DACK2
A27	SA4	B27	TC
A28	SA3	B28	BALE
A29	SA2	B29	+5V
A30	SA1	B30	OSC
A31	SA0	B31	GND
A32	GND	B32	GND

Table 18: PC/104 8-bit Interface

16-bit, 40-pin Connector (CN13)

PC/104 16-bit Connector (CN13)			
Pin #	**Signal**	**Pin #**	**Signal**
C0	GND	D0	GND
C1	/SBHE	D1	/MEMCS16
C2	LA23	D2	/IOCS16
C3	LA22	D3	IRQ10
C4	LA21	D4	IRQ11
C5	LA20	D5	IRQ12
C6	LA19	D6	IRQ15
C7	LA18	D7	IRQ14
C8	LA17	D8	/DACK0
C9	/MEMR	D9	DRQ0
C10	/MEMW	D10	/DACK5
C11	SD8	D11	DRQ5
C12	SD9	D12	/DACK6
C13	SD10	D13	DRQ6
C14	SD11	D14	/DACK7
C15	SD12	D15	DRQ7
C16	SD13	D16	+5V
C17	SD14	D17	/MASTER
C18	SD15	D18	GND
C19	GND(*)	D19	GND

Table 19: PC/104 16bit Interface

4.9 SO-DIMM Socket (CN15)

The SO-DIMM memory socket accommodates one industrial standard 144-pin SO-DIMM memory module. The memory type compatible with the MZ104 is 32-bit, 3.3V PC100 or PC66 SDRAM. The MZ104 can handle a maximum of 128MB of SDRAM[3]. The BIOS automatically senses the amount of memory installed in your system and saves that information in the CMOS SETUP memory when you save the SETUP information. For further information on MZ104+ Memory, please refer to Appendix 1 of this manual.

Note: The ZFx86 processor on the MZ104+ is a 32-bit processor thereby requiring 32-bit SO-DIMM memory modules.

MZ104+ SDRAM SO-DIMM modules (8 - 64MB) are available from Tri-M Systems.

Part number: MEM-XXMB-MZ (XX = capacity in MB)
Example: MEM-32MB-MZ is a 32MB module

[3] Maximum available in a standard size SO-DIMM module is 64MB. For 128MB, an oversized card must be used. This is currently not available from Tri-M Engineering.

4.10 WATCHDOG TIMER (CN16)

The ZFx86 chip on the MZ104 offers two watchdog timers, WD1 (16-bit counter) and WD2 (8-bit counter). Both timers are programmable. The maximum period for WD1 is two seconds while the maximum period for WD2 is 7.2ms. WD2 starts counting down after WD1 expires. When WD2 counter reaches zero, it will unconditionally cause system reset.

The watchdog timer will alarm if not triggered by the system or application at least once every 2 seconds. If the watchdog timer does not receive its reset ("tickle") after 2 seconds has elapsed, it generates its alarm signal. The watchdog timer alarm is reset ("tickled") by toggling the WDI signal or writing to index 0x10h of the ZF-Logic I/O space. The watchdog is triggered continuously (disabled) if jumper is installed at 2-3 of CN16. This arrangement allows watchdog input (WDI) be toggled by watchdog alarm output (WDO) in a self-triggering fashion. If jumper is installed at 1-2 of CN16, the watchdog will be triggered by an external signal from pin12 of CN7. You must provide this trigger signal.

Jumper Position	Function
1-2	External source to reset watchdog
2-3	Disable watchdog

Table 20: Watchdog Jumper

The watchdog timer alarm signal (WDO) can be programmed to generate the following response when corresponding bit is set at the watchdog control register in the ZF-Logic I/O space.

- Non-maskable interrupt (NMI)
- System controller interrupt (SCI)
- System Management interrupt (SMI)
- Hardware reset

For further information on the Watchdog Timer and for programming detail, please consult the ZFx86 data book provided on the MZ104 Quickstart CD and available for download at www.zfmicro.com.

Note: The watchdog timer is not enabled at power up by the BIOS. Therefore, when the jumper is installed at CN16 it does not affect the operation of the MZ104.

4.11 DiskOnChip SOCKET (IC23)

The MZ104 provides a 32-pin DIP socket, which can be populated with either an M-Systems' DiskOnChip 2000 and DiskOnChip Millennium product. Before the DiskOnChip can be accessed, the memory windows, which the socket is mapped to, must be enabled. This is accomplished by the ISA memory parameters in the CMOS setup. Please consult the **ZFx86**

BIOS Supplement manual for detailed explanation on setting up memory windows. To enable the socket, please follow the steps below:

1. Enter CMOS setup by pressing function key **F2** prior to booting OS from boot media.
2. From the menu bar of the **Main** setup screen, choose **Advanced**.
3. From the **Advanced Setup Screen**, choose **Advanced Chipset Control**.
4. Set **Onboard RFD** to **Disabled**.
5. From **Advanced Chipset Control**, choose **ISA Memory chip select setup**
6. Set **Memory Window_Mem_CS3** as follows:
   - Window Size: 1
   - Window Base: D0
   - Window Page: F30
   - Window Data Width: 8-Bit
7. Save setup & exit
8. Reboot computer

Note: The memory window setting is lost when the MZ104+ is powered down unless a backup battery is provided. Use ZF Micro Devices' ZEB utility to set defaults into the BIOS. ZEB utility is provided in the BIOS folder on the MZ104 quickstart CD and is also available for download at www.zfmicro.com

Pin Name	Description	Pin Number	Direction
A0 – A12	Address bus	4-12, 23, 25-27	Inputs
D0 – D7	Data bus	13-15, 17-21	I/O
CE/	Chip Enable	22	Input
OE/	Output Enable	24	Input
WE/	Write Enable	31	Input
NC	Not Connected	1, 2, 3, 28, 29, 30	
VCC	Power	32	
GND	Ground	16	

Table 21: DiskOnChip Socket (IC23)

CHAPTER 5 – SETUP

5.1 MZ104 INTERRUPT AND I/O PORT ASSIGNMENTS

IRQ Number	MZ104 Assignment
0	Systems timer (not available for other devices)
1	Keyboard controller (not available for other devices)
2	Second PIC cascade (not available for other devices)
3	Serial port two (COM2:)
4	Serial port one (COM1:)
5	Unassigned
6	Floppy Disk controller (not available for other devices)
7	Parallel (printer) port one (LPT1:)
8	Real-time clock (RTC)
9	Unassigned
10	Unassigned
11	USB
12	PS/2 Mouse
13	Math coprocessor
14	Primary IDE
15	unassigned

Table 22: MZ104 Interrupt Assignments

I/O Address	Hardware
0000 - 000F	DMA Controller
0020 – 0021	PIC
0022 – 0021	Motherboard Resources
0040 – 0043	System Timer
0060 – 0060	Keyboard
0061 – 0061	Systems Speaker
0064 – 0064	Keyboard
0070 – 0071	System CMOS / Real time clock
0081 - 008F	DMA Controller
0092 – 0092	Motherboard Resources
00A0 - 00A1	PIC
00C0 - 00DF	DMA Controller
00F0 - 00FF	Numeric Data Processor
02F8 - 02FF	Communications Port B
0378 - 037F	Printer Port
03F0 - 03F5	Floppy Disk Controller
03F7 - 03F7	Floppy Disk Controller
03F8 - 03FF	Communications Port A
0480 - 048F	Motherboard Resources
04D0 - 04D1	Motherboard Resources
0778 - 077F	Printer Port
0CF8 - 0CFF	PCI Bus
AC00 - AC1F	Motherboard Resources
AC80 - AC9F	Motherboard Resources

Table 23: MZ104 I/O Port Assignments

5.2 BIOS SETUP

The MZ104 system BIOS (Basic Input Output System) supports a standard SETUP function to configure system parameters. The BIOS uses these parameters to establish default conditions during system initialization, both during the Power On Self Test (POST) phase, and during system boot.

Using SETUP

To enter the SETUP function, press the <F2> key during POST.

Note: When you change SETUP parameters, the new values do not take effect until the system is rebooted.

For details about how to set the various parameters using SETUP, please refer to the MachZ BIOS Users Manual Supplement and the PhoenixBIOS 4.0 Rev 6 manual provided on the MZ104 Quickstart CD or available for download at www.ZFLinux.com.

APPENDIX 1 – MZ104 MEMORY INFORMATION

The ZFx86 processor on the MZ104, like other X'86 processors, requires "main memory". The main memory of the ZFx86 must be SDRAM (Synchronous Dynamic Random Access Memory). The SDRAM controller of the ZFx86 can access SDRAM chips with densities from 16Mbit to 128Mbit.

Tri-M Engineering uses a modular memory approach with the MZ104, thus allowing customers to select the size of memory that best fits their application. Standard DIMM modules are not used, as they are physically too large to fit the PC/104 footprint of the MZ104. Similarily, 72-pin SO-DIMMS are not used as the connectors are increasingly difficult to source primarily because laptop computers have moved to the 144-pin SO-DIMMS. The problem that arises with the common laptop 144-pin SO-DIMMS is that they are designed for 64-bit processors whereas the ZFx86 can handle a maximum of 32-bit. This means that either only half the memory can be utilized, or "custom" memory cards are required. Some of the standard memory cards on the market can be "depopulated", thus not requiring the manufacturer to produce a custom PCB. However, not all SO-DIMM memory cards can be depopulated and still work with the ZFx86. When SDRAM chips of 16-bit width are used, some manufacturers wire the one half of the memory into the second 32-bit. This makes for an efficient PCB layout, but when a chip is depopulated, it also depopulates the lower 32 bits. The lower 32-bits are the ones the ZFx86 processor requires.

Note: For those who wish to manufacture their own SDRAM SO-DIMM memory modules, Tri-M Engineering will supply the schematics and Gerber files upon request free of charge.

APPENDIX 2 - LITERATURE REFERENCES

The following references are for information about the PC/104 architecture, the PC DOS, and the PC BIOS.

ISA System Architecture

MindShare, Inc., Tom Shanley and Don Anderson
Internet: mindshar@interserv.com
CompuServe: 72507,1054
Published by Addison Wesley, Inc.

AT Bus Design

Edward Solari
Anabooks
12145 Alta Carmel Ct., Suite 250
San Diego, CA 92128
ISBN 0-929392-08-6

Personal Computer Bus Standard P996

Institute of Electrical and Electronic Engineers, Inc.
445 Hoes Lane
Piscataway, NJ 08854

PC Interrupts

PC Interrupts, Ralf Brown, Addison/Wesley.

BIOS Reference

System BIOS for IBM PC/XT/AT Computers, Phoenix, Addison/Wesley

PC/104 Consortium

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Mountain View, CA 94040
Phone: 415 903-8304
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